

IN THE CLAIMS:

None of the claims have been amended herein. All of the pending claims 1 through 14 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Original) A transistor, comprising:

a substrate;

a nitrogen-free polysilicon electrode contacting a portion of the substrate; and

a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including about 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

2. (Previously presented) The transistor of claim 1, wherein the nitrogen-free polysilicon electrode has a bottom surface comprising a P-type dopant.

3. (Original) The transistor of claim 2, wherein the P-type dopant is boron.

4. (Original) A surface P-channel transistor, comprising:
a substrate;
a nitrogen-free polysilicon electrode contacting a portion of the substrate, the electrode
comprising a P-type dopant including boron; and
a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate
oxide including about 0.5% nitrogen by atomic weight at an interface with the substrate,
the nitrogen progressively increasing to comprise between 2.5% and 10.0% nitrogen by
atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide
hardened using a remote plasma-based nitrogen hardening treatment and annealed
thereafter.

5. (Previously presented) The surface P-channel transistor of claim 4, wherein the
gate oxide comprises a hardened gate oxide using the remote plasma-based nitrogen hardening
treatment using a high density plasma process for approximately 60°C for about 10 seconds using
about 1500 watts of power.

6. (Previously presented) The surface P-channel transistor of claim 4, wherein the
gate oxide comprises hardening the gate oxide using a thermal remote plasma-based nitrogen
hardening treatment process at approximately 750°C for about 2 minutes.

7. (Previously presented) The surface P-channel transistor of claim 4, wherein the
gate oxide comprises a hardened gate oxide annealed at approximately 800°C for
approximately 60 seconds.

8. (Previously presented) A transistor, comprising:
a substrate;
a nitrogen-free polysilicon electrode contacting a portion of the substrate; and
a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including essentially 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise essentially in the range of between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

9. (Previously presented) The transistor of claim 8, wherein the nitrogen-free polysilicon electrode has a bottom surface comprising a P-type dopant.

10. (Previously presented) The transistor of claim 8, wherein the P-type dopant includes boron.

11. (Previously presented) A surface P-channel transistor, comprising:
a substrate;
a nitrogen-free polysilicon electrode contacting a portion of the substrate, the electrode comprising a P-type dopant including boron; and
a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including essentially 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise essentially in the range of between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

12. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide using the remote plasma-based nitrogen hardening treatment using a high density plasma process for essentially 60°C for about 10 seconds using essentially 1500 watts of power.

13. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises hardening the gate oxide using a thermal remote plasma-based nitrogen hardening treatment process at essentially 750°C for essentially 2 minutes.

14. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide annealed at essentially 800°C for essentially 60 seconds.